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09/675,209	09/29/2000	Mikimasa Suzuki	1-85	3030

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EXAMINER
FARAHANI, DANA

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 07/26/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Application No. 09/675,209	Applicant(s) SUZUKI ET AL.
	Examiner Dana Farahani	Art Unit 2814

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 May 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20 and 38-51* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20 and 38-51* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Claims 1-20, 38, and 39 in Paper No. 6 is acknowledged.

Claim Objections

2. Claim 11 is objected to because of the following informalities: on line 4, the word "gat" should be "gate". Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 2, 7, 40-42, 46, 48-51, are rejected under 35 U.S.C. 102(b) as being anticipated by Kinzer (U.S. 5,644,148), previously cited.

Regarding claim 1, Kinzer discloses, figure 19, a semiconductor substrate 52; a plurality of cell blocks provided on the semiconductor substrate; a plurality of gate electrodes G electrically independent of one another and respectively provided in the plurality of cell blocks; and a plurality of gate pads (not shown) are provided on the semiconductor substrate and respectively connected with the plurality of gate electrodes (see column 12, lines 60-65).

Regarding claim 2, see figure 18.

Regarding claim 7, the semiconductor substrate is an insulated gate type bipolar transistor chip.

Regarding claim 40, disclosed in figure 2 is a plurality of transistor cells arranged in a semiconductor chip and divided equally into a plurality of groups; a plurality of common gate electrodes G for the plurality of groups, respectively; and a plurality of gate pads for the plurality of common gate electrodes, respectively (see column 6, lines 42-44).

Regarding claims 41 and 51, see figure 2, wherein source electrode 40 is an emitter electrode and drain electrode 41 serves as a collector.

Regarding claims 42, 46, and 48-50, the claims recite a source potential is applied to the equipotential pad, and equipotentail pad is provided for the gate pad. Therefore, the only structural limitation in this claim is a plurality of pads adjacent to the gate pads. Disclosed in figure 2 a pad, not numbered, on top of element 40, at the most left had side of the figure, is adjacent to the plurality of gate pads (not shown).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 3 and 16-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kinzer, as applied to claims 1 and 2 above, and further in view of Smith (U.S. 6,329,692), and further in view of Kohno et al., hereinafter Kohno (U.S. 6,180,966), all previously cited.

Regarding claim 3, Kinzer discloses the claimed invention except for a ground and a gate terminal to be connected to the semiconductor device.

Smith discloses, figure 4, a ground terminal Vss and a gate terminal VDD, electrically independent of the ground terminal, where the gates of the transistors 42 and 36 connected to those terminals, respectively. Kohno discloses plurality of cell blocks, as shown in figure 2, in which the over current can damage the cells. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to include Smith's over voltage protection circuit in the structure Kinzer discloses in order to protect the circuit from over voltage and over current.

Regarding claim 16, Smith discloses the emitter potential 32 of figure 3 is on the semiconductor substrate. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to include this potential in order to power the device.

Regarding claim 17, Kinzer discloses, in figure 2, the pads are connected with cell blocks shown in the figure (see column 6, lines 38-47).

Kinzer does not disclose gate terminal outside of the substrate connected to the cell blocks.

Smith discloses gate 24 has a terminal outside of the substrate. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to include the terminal in the structure Kinzer discloses in order to provide the gate with a potential.

Regarding claims 18 and 19, Kinzer discloses, figure 22, a plurality of emitter electrodes respectively provided in the plurality of cell blocks (shown in figure 1); a plurality of emitter pads, not numbered, below the emitter electrodes; and a collector electrode 302 provided on a back surface of the semiconductor substrate. Although Kinzer does not disclose emitter and collector terminals, it would have been obvious to one of ordinary skill in the art at the time of the invention to provide the terminals in order to provide necessary voltage for the collector and the emitter, and further encapsulate the terminals in a resin member in order to be able to see inside of the terminals.

7. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kinzer, as applied to claim 1 above, and further in view of Sanchez (U.S. 6,160,305), previously cited.

Kinzer discloses the claimed invention except for an emitter pad and a source pad with the connection the applicant discloses.

Sanchez discloses, figure 1, gate terminal of transistor 20, shown as OUT in the figure, and an emitter terminal of transistor 12, shown with an arrow, to have an emitter potential, and a source pad connected to the emitter. Therefore, it would have been

obvious to one of ordinary skill in the art at the time of the invention to include this thermal sensing structure in Kinzer in order to protect it from over heating.

8. Claims 8-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kinzer, as applied to claim 1 above, and further in view of Calhoun (U.S. 4,631,569), previously cited.

Regarding claims 8-10, 13, and 15, Kinzer discloses the claimed invention except for a plurality of marks provided at a plurality of regions of the semiconductor substrate for determining the defectiveness of the particular cells.

Calhoun discloses plurality of circuit cells in which the defective cells are marked to be distinguished from the working cells (see column 4, lines 25-48). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to mark the defective cell blocks to discriminate them from the working cell blocks.

Regarding claims 11, 12, 14, it would have been obvious to provide the mark on a line passing through the gate pad, since the gate pad has a large area.

9. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kinzer and further in view of Smith, and further in view of Kohno as applied to claim 16 above, and further in view of Shinohe et al., hereinafter Shinohe (U.S. 5,793,065), all previously cited.

Kinzer in view of Smith and Kohno discloses the claimed invention except for the different threshold voltages of adjacent group of cells.

Shinohe discloses the use of adjacent elements having different threshold voltages reduces the adverse influence of threshold voltage difference among the

elements (see column 44, lines 62-66). Therefore, It would have been obvious to one of ordinary skill in the art at the time of the invention to make the threshold voltages different in order to reduce the adverse influence of threshold voltage difference among the neighboring elements.

10. Claims 38 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kinzer in view of Smith, and further in view of Crane, Jr. et al., hereinafter Crane (U.S. 6,339,191), previously cited.

Kinzer disclose, figures 1 and 2, a plurality of chips, each having a semiconductor substrate 20, a plurality of cell blocks provided on the semiconductor substrate, a plurality of gate electrodes G electrically independent of each other, and gate pads, not shown in the figure, connected with the gate electrodes.

Kinzer does not disclose gate pad connected to emitter or ground potential.

Smith discloses, figure 4, gate of transistor 42 connected to ground, and gate of transistor 36 connected to a voltage potential. Crane discloses trays to carry dies (see column 24, lines 50-55). Therefore, It would have been obvious to one of ordinary skill in the art at the time of the invention to make the gate connections to the ground and a voltage in order to disable and enable the cells, respectively; and further use trays in order to carry the chips.

11. Claims 43-45 and 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kinzer.

Regarding claims 43 and 45, Kinzer discloses in figure 2 gate terminal G, a source terminal connected to the upper left hand side of source electrode 40, and drain terminal connected to the bottom drain electrode 41.

Kinzer does not disclose, in figure 2, gate terminal is connected to some of the gate pads.

Kinzer discloses in figure 19, gate terminal G is connected to some of the gate pads. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to connect the gate terminal to some of the gate pads in order to be able to control each transistor separately.

Regarding claims 44 and 47, Kinzer discloses the claimed invention except an encapsulating resin. It would have been obvious to one of ordinary skill in the art at the time the invention was made to encapsulate the semiconductor chip, the wires, part of the gate terminal, and part of the drain terminal, since it was known in the art that such encapsulation is used to encapsulate semiconductor chips.

Product-by-Process Limitations

While not objectionable, the Office reminds Applicant that "product by process" limitations in claims drawn to structure are directed to the product, per se, no matter how actually made. *In re Hirao,* 190 USPQ 15 at 17 (footnote 3). See also, *In re Brown,* 173 USPQ 685; *In re Luck,* 177 USPQ 523; *In re Fessmann,* 180 USPQ 324; *In re Avery,* 186 USPQ 161; *In re Wethheim,* 191 USPQ 90 (209 USPQ 554 does not deal with this issue); *In re Marosi et al.,* 218 USPQ 289; and particularly *In re Thorpe,* 227

USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or otherwise. Note that applicant has the burden of proof in such cases, as the above case law makes clear. Thus, no patentable weight will be given to those process steps which do not add structural limitations to the final product.

For example, in claims 4 and 6, the gate pad is bonded to the gate terminal by "one of wire-bonding, soldering, and pressure-welding" is considered methods of forming the base region and not limitation of the final product. Therefore, such limitations are given no patentable weight.

Response to Arguments

12. Applicant's correction to the claims is acknowledged, and therefore, the claim objection is withdrawn.

13. Applicant's arguments filed on 5/30/02 have been fully considered but they are not persuasive.

Regarding applicant's argument that the limitation "gates of the cells are independent form each other" is not found in any of the references is not found persuasive.

Kinzer discloses in figure 19 the gate output terminal (G) is separated from the adjacent gates. A reference is good for everything it discloses. Therefore, each gate is

independent from the adjacent gates, and can operate independently since the gates are not connected to each other, as shown in the figure.

Regarding applicant's argument that "Shinohe discloses that the use of adjacent elements having different threshold voltages reduces the adverse influence of threshold voltage differences among the elements....This feature is different from that recited in claim 20" is not persuasive.

Claim 20 states "...the plurality of cell blocks includes a first group of cell blocks having an equal threshold voltage and connected with the gate terminal, and a second group of cell blocks having different threshold voltages from one another...". Therefore, it was appropriate to make an obviousness rejection in view of Shinohe reference.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dana Farahani whose telephone number is (703)305-1914. The examiner can normally be reached on M-F 8:00AM - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (703)306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are (703)872-9318 for regular communications and (703)872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Dana Farahani
July 21, 2002

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